

a²
cont
a encryption engine coupled to said bus to encrypt signals transferred from said receiver to said bus, said encryption engine to provide two different levels of encryption; and

a decryption engine coupled to said bus to decrypt signals transferred from said bus to said display.

a³
13. (Amended) The bus of claim 11 wherein said bus is adapted to periodically encrypt at a higher level of encryption.

a⁴
14. (Amended) The bus of claim 13 wherein the level of encryption is adapted to change on frame boundaries.

a⁴
23. (Amended) The platform of claim 22 wherein one of said slots is coupled to receive a motherboard with a processor.

a⁵
26. (Amended) The platform of claim 25 wherein said encryption levels are changed periodically.

Remarks:

A. Rejection Under 35 U.S.C. § 112

Claim 26 has been amended to depend from claim 25, and thus claim 26 has sufficient antecedent basis.

B. Rejection of Claims Under 35 U.S.C. § 102

Pending claims 1-3, 5-10, 22-23 and 28 stand rejected under 35 U.S.C. § 102(e) over U.S. Patent No. 6,137,539 to Lownes. Applicants respectfully traverse the rejection. With regard to claim 1, Lownes does not disclose, at least, a digital graphics bus coupled to a receiver in a first housing and a display in a second housing. In this regard, Lownes shows only a bus